Efficient Methods for Analyzing the Floating Diffusion, Photodiode, and Transfer Gate of a 4T Pixel and Calibrating TCAD

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***Abstract*—A two-step approach is presented for investigating the electrical properties and behavior of 4T pixels through measurements and simulation. Using this methodology, key pixel parameters such as the pinning voltage, barrier potential, floating diffusion (FD) swing characteristics, and full well capacity are assessed. The first method focuses on the FD response in an active image sensor array, while the second method investigates the electrostatic potential in a dedicated test structure. By correlating experimental data with TCAD simulations, the study reveals how the electrostatics influence pixel behavior under varying conditions, and how TCAD accuracy can be improved through doping profile calibration. The results offer a deeper understanding of 4T pixels, improving predictive modeling and supporting the development of advanced pixel architectures.**

***Index Terms*—4T pixel characterization, TCAD simulation**

I. Introduction

A 4T pixel consists of a pinned photodiode (PPD) and a floating diffusion (FD), connected by a transfer gate (TX). The design and operation of such a pixel are well-understood [1], and schematically presented in Figure 1. The PPD's doping profile forms a depleted well with a fixed maximum potential, called the pinning voltage. During the exposure time, generated electrons accumulate in this well. When the TX is pulsed, the charges are transferred from the PPD to the FD, resulting in a reduction of the FD voltage corresponding to the signal level. Before each transfer, the FD is reset to a high voltage using a reset transistor (RST). The FD level is read out with a source follower (SF) and select transistor (SEL), transferring the voltage onto a column bus (COL).

One of the key advantages of 4T pixels is their ability to operate in correlated double sampling (CDS) mode, which reduces noise. In CDS, each pixel's FD is sampled twice: the first time after reset (sample reset, SR) and the second time after charge transfer from the PPD (sample signal, SS). By subtracting SR from SS, the signal corresponding to the transferred electrons is isolated, and the thermal reset noise is effectively canceled. Furthermore, the pinned nature of the PPD structure helps suppress dark current. Overall, the 4T pixel architecture enables low-noise readout and efficient charge transfer, making it a dominant choice for modern CMOS image sensors.

The performance of a 4T pixel is described by various high-level parameters such as full well capacity (FWC), conversion gain (CG), linearity, and noise—extracted from response curves. These parameters are linked to key properties of the pixel, such as the pinning- and TX-barrier potentials (φ_{pin} and $\varphi_{barrier}$, respectively). Various pixel-level characterization methods exist for investigating these features and correlating the results with analytical models

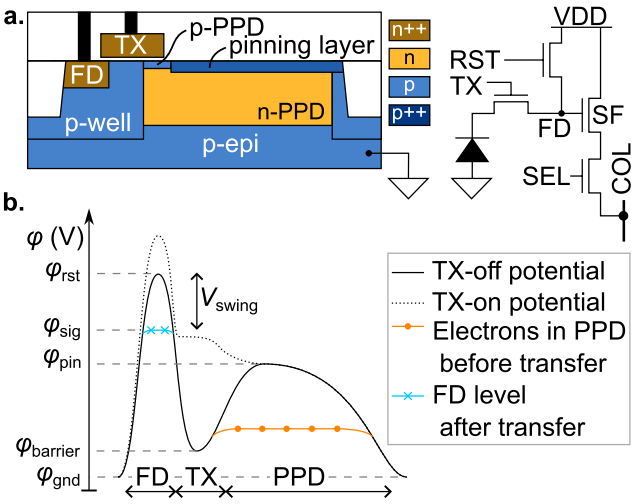

Fig. 1: **a.** Schematic and doping profile of a 4T pixel. **b.** Electrostatic potential diagram and illustrative filling levels when TX is off and on.

and TCAD [2]–[4]. Generally, these methods focus on gaining insight into the PPD and TX. However, it can be equally important to look at the effects of the FD on performance. Experimentally probing the FD of pixels is non-trivial, because the readout generally passes through a SF, column bus, and various circuits, introducing a non-linear gain and spatial noise.

This study presents a two-step measurement approach, building upon the existing literature, in which analysis of the PPD and TX is combined with pixel-level investigation of the FD in 4T pixels. By aligning measurements with TCAD simulations, we aim to enhance simulation accuracy and provide a more comprehensive understanding of 4T pixels. The proposed methodology offers a practical framework for evaluating pixels in a simple yet extensive way, thereby aiding in the development of next-generation image sensors with improved performance.

II. Methodology

Two characterization methods are discussed to help in the analysis of the FD, PPD, and TX-barrier of pixels, starting with a method for the FD.

A. Floating diffusion

The voltage on the FD at different stages of operation provides insights into the pixel's reset behavior, linearity, and swing characteristics. To accurately determine this voltage, we propose a method that repurposes the sampling circuitry natively present in the sensor, as well as black clamps on the column buses. The typical use of the clamps

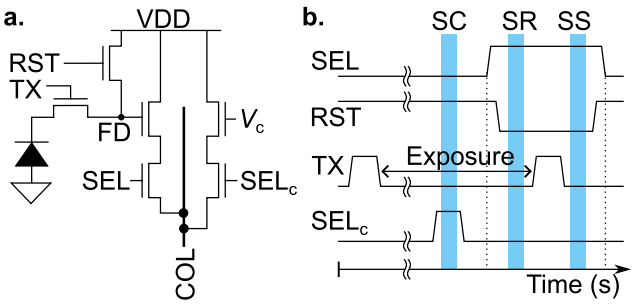

Fig. 2: **a.** Pixel schematic, including a black clamp on the column. **b.** Timing diagram showing the sampling of the clamp (SC), reset (SR), and signal (SS) levels.

is to limit column voltage variations and ensure stable sensor operation.

The black clamps are implemented with SF and SEL transistors identical to those of regular pixels. This way, the clamp can drive a voltage onto the column bus in the same manner as a regular pixel, using select transistor SEL_c. In other words, the clamp input V_c has an equivalent role as the FD of a pixel. By separately enabling the select transistor of the clamp and a pixel, the difference in their response on the column can be measured. The value of V_c can then be identified for which the two responses are identical, corresponding to an accurate estimate of the FD voltage in the selected pixel.

In practice, the sample-and-hold circuitry responsible for capturing the reset- (SR) and signal levels (SS) can be used for this comparison. A typical timing diagram for a single pixel is shown in Figure 2. The column voltage is first sampled when the clamp is enabled (SC), and subsequently sampled again when the selected pixel is read out at SR or SS. By sweeping the clamp input voltage and identifying the zero-crossing point where the difference between the two sampled values is minimal, the corresponding FD voltage can be determined. The clamp-based voltage comparison method reduces many readout-induced non-idealities, enabling a practical characterization of the FD voltage in 4T pixels. However, the accuracy of the extracted voltage is limited by SF and SEL transistor variations between the clamp and pixels, as well as the difference in voltage drops over the column.

B. Photodiode and transfer gate

The second method involves evaluating the pinning voltage and transfer barrier potential of the PPD using a dedicated test device, referred to as a Vpin structure, as shown in Figure 3.a. (It should be noted that various equivalent methods exist to obtain similar results, including methods where no dedicated structure is required [3].) The device in this work consists of a pixel in which an additional contact is placed on the PPD. A small current I_{ppd}, in the order of $-100\,pA$, is sourced through the contact, while the FD is biased at a fixed potential near the reset voltage. The voltage on the PPD contact reflects the photodiode's potential and depends on the TX bias. By measuring this voltage, key information about the PPD and TX can be extracted.

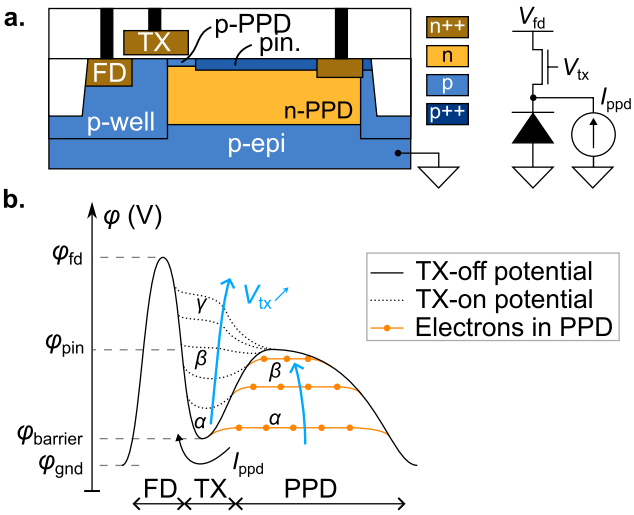

Fig. 3: **a.** Schematic and doping profile of a Vpin structure. **b.** Electrostatic potential diagram versus TX bias.

Figure 3.b schematically illustrates the PPD potential as a function of TX bias. When the TX is closed (state α), the current source fills the PPD potential well with electrons until they diffuse over the TX barrier and overflow into the FD. The resulting voltage measured at the PPD contact is strongly linked to the barrier potential $\varphi_{barrier}$. As the TX opens, the filling level of the PPD decreases along with the potential below the TX (state β). This trend continues until the channel potential exceeds the pinning potential φ_{pin}, at which point the PPD can no longer store carriers. The externally measured voltage now saturates at the so-called pinning level (state γ). $\varphi_{barrier}$ and φ_{pin} determine the ability of a photodiode to accumulate generated charges—affecting saturation FWC and other pixel metrics.

The potential diagram in a pixel is largely determined by the doping profile and biasing conditions of the device. Hence, the various features of the doping, shown in Figure 1.a, play a key role in device behavior [4]. Sometimes, measurements of real devices can deviate from simulation results. In this case, the numerical results can be re-aligned by improving the calibration of the process conditions and doping profile in TCAD. An example of such calibration is given in the next section.

On another note, accurately measuring and predicting the saturation FWC is key for assessing pixel performance. To ensure that measurements and simulations of FWC are comparable, it is essential to employ consistent methodologies that reflect the underlying charge transport physics. Specifically, when the PPD accumulates charges under illumination, excess carriers may overflow via paths with the lowest potential barriers—typically below TX. This temperature-dependent process continues until an equilibrium is reached, where the photogeneration rate equals the leakage rate [5]. Simulations must replicate these illumination and overflow conditions to ensure that the simulated FWC aligns with real-world measurements. A reasonable set-point for the light intensity is the point where enough carriers are generated to completely fill the PPD during an exposure time equal to the inverse of the sensor's frame rate.

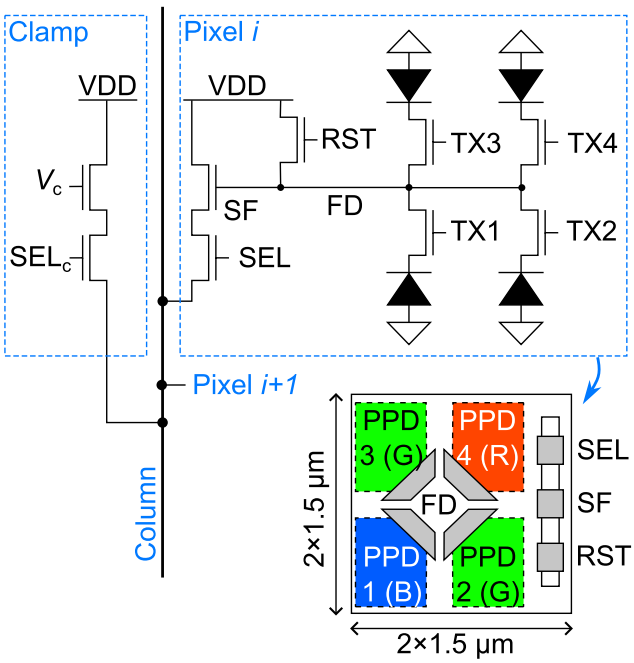

Fig. 4: Schematic of a 2×2 shared 4T pixel connected to a column bus with a black clamp.

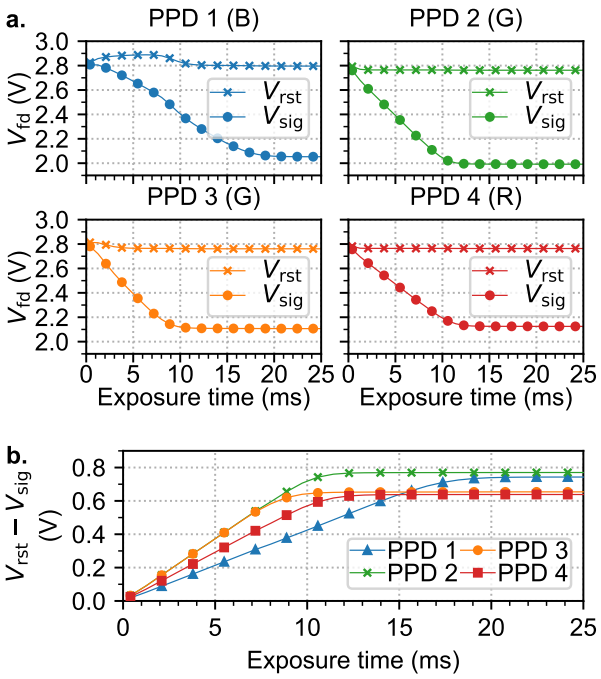

Fig. 5: **a.** Reset- and signal FD voltages versus exposure time for continuous white-light illumination. **b.** Corresponding FD swing curves.

III. Method Validation & Results

The FD, PPD, and TX-barrier of the pixels in a small sensor and a corresponding Vpin structure are characterized using the previously discussed methods.

A. 2×2-shared 4T pixel

The sensor contains 2×2-shared 4T pixels with 1.5 µm pitch and a Bayer color filter array (CFA), as shown in Figure 4. Due to its relative simplicity compared to more advanced pixel architectures, this design provides a good platform for gaining insight into the sensor process technology, and measurement results can be efficiently aligned with TCAD using process information provided by the foundry. Moreover, the pixel symmetries offer a unique opportunity for investigating process details that other 4T pixels cannot unveil.

The sensor is integrated with a set of default process conditions, referred to as the *Reference*. In addition, chips are available for which specific elements of the process flow have been modified to investigate the effect on device performance. These split conditions can be summarized as follows:

(a) *P-type TX*: The doping of the TX gates is changed from n- to p-type, shifting the work function.
(b) *Barrier↓*: The barrier potential below the TX is slightly weakened, increasing leakage.
(c) *P-well* Δ: The p-well is deepened, increasing leakage.
(d) *Vpin↑*: The pinning voltage is increased, improving charge-storing capability.

Sometimes, multiple orthogonal split conditions are combined into one integration scheme.

B. Floating diffusion

Each column in the sensor array contains a clamp consisting of SF and SEL transistors identical to those of regular pixels. The clamp input voltage can be accurately selected through an on-chip resistor ladder. Using the methodology of Section II-A, the clamps are exploited to determine the FD voltages during the sample reset (V_{rst}) and sample signal (V_{sig}) states of each sub-pixel (1 to 4) in the sensor.

Figure 5.a. presents the average results of the four PPDs in a 2×2-shared pixel as a function of exposure time when uniformly illuminated with white light. All split conditions behave similarly here, so only devices with the *Reference* condition are discussed. For each diode, the reset voltage is close to 2.8 V and relatively independent of exposure time. However, a notable exception is found for PPD 1, where V_{rst} deviates at integration times below 10 ms. This offset is attributed to the timing of the shared pixel. Specifically, the timing is designed so that the exposure of each PPD starts and ends in sequence, with one line time between each diode. Therefore, the PPD1 in a shared cell receives notably different (soft) reset conditions compared to PPD2–4.

The FD response gives insight into the behavior of an individual pixel, including reset and saturation. Additional information can be extracted by subtracting the voltages $V_{rst} - V_{sig}$, as shown in Figure 5.b. This response reveals how the FD swing varies with exposure, and it can be used to analyze CG, linearity, and saturation behavior. Due to the CFA, the illumination intensity varies for each photodiode, altering the slopes of the response curves. Moreover, the pixels saturate at different levels in a range from 0.64 V to 0.77 V. The origin of this difference is twofold: (a) varying illumination intensities and (b) spatial non-uniformity in doping. The latter is amplified by the point symmetry of the shared pixels.

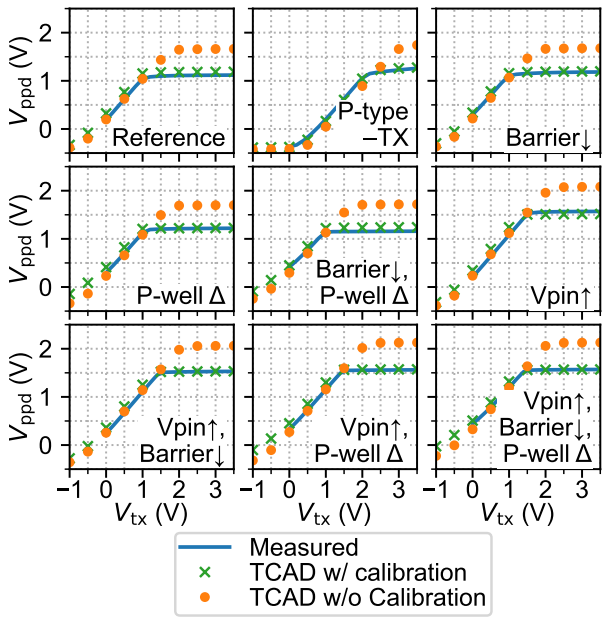

Fig. 6: Vpin structure measurement and simulation results, before and after TCAD calibration, for different process conditions ($I_{ppd} = -100\,\text{pA}$, $V_{fd} = 2.9\,\text{V}$).

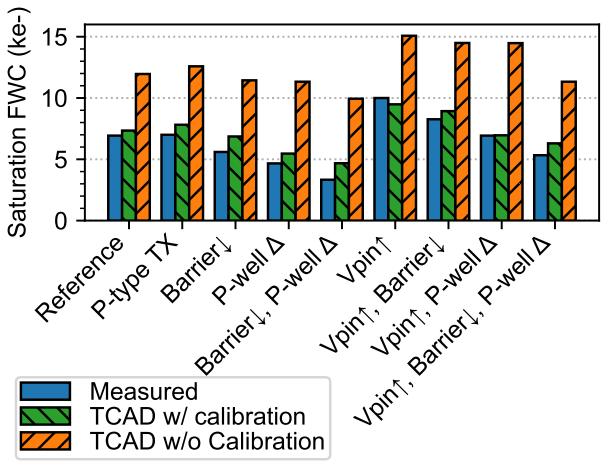

Fig. 7: Average saturation FWC measurement and simulation results, before and after TCAD calibration, for different process conditions.

C. Photodiode and transfer gate

The PPD and TX are characterized using a dedicated test structure as described in Section II-B. A contact is placed on the PPD at a large distance from TX to minimize the effect on the electrostatic potential close to the transfer gate. A voltage of $2.9\,\text{V}$ is applied to the FD contact, and a constant current of $-100\,\text{pA}$ is sourced through the PPD contact. The test is conducted by sweeping the TX bias and measuring the PPD voltage on physical devices. In addition, the test is recreated in TCAD.

Figure 6 shows the measured response curves and corresponding simulation results for different process splits. In all cases, the PDD potential gradually slopes upwards as TX is opened and saturates at the pinning level. Moreover, the results are in line with expectations when specific process conditions are changed. The measured curves predict pinning levels of $\approx 1.2\,\text{V}$ and $1.55\,\text{V}$ for splits with *Reference* and *Vpin↑* conditions, respectively. Additionally, the curves are shifted by $\approx 1\,\text{V}$ when the TX-doping type is swapped.

The figure also shows the simulated response for two cases: (a) using only the information provided by the foundry, and (b) with some additional process-specific calibration of the doping profile. The calibration is done by tuning doping elements in an attempt to reproduce the various features of the measured test curves. Moreover, the calibration is kept consistent across all splits. Specifically, the p+ pinning layer is modified to reduce the pinning level. Additionally, the p-PPD doping at the entry of the TX gate is adjusted to match the slope offsetting the curves. Finally, the p-well below the TX gate is adjusted to match the barrier potential when the TX is off. Using these modifications, an electrostatic potential is obtained in simulation that more faithfully represents physical devices. This allows for a better understanding of the behavior and identifying points of improvement.

Finally, the saturation FWC is investigated, using the insights of Section II-B. Figure 7 shows the saturation FWC as measured and simulated for different split conditions. In the absence of additional doping calibration, the simulation overestimates the pinning voltage and barrier potential, resulting in FWC predictions that exceed those observed in real devices—typically by 4–6ke-. When applying the process modifications discussed in the previous paragraph, a closer match is found between measurements and simulations for all split conditions. This result provides further confidence that the methods can be applied beyond the scope of this study, for example, in the design of new pixels using the same process technology.

IV. Conclusion

The proposed methods provide an effective way to validate pixels and improve the predictability of TCAD—achieving a good match between experiments and simulations after calibration for a test pixel. Moreover, by leveraging existing black clamp circuitry on the columns in image sensors, minimal additional design effort is required to employ them. The insights gained from the analysis of the established 4T shared-FD device are of great use in the design of more advanced pixel architectures.

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